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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/588,103	07/31/2006	Mineo Miura	AI 420NP	4037

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EXAMINER	
YEUNG LOPEZ, FEIFEI	
ART UNIT	PAPER NUMBER
2826	

MAIL DATE	DELIVERY MODE
01/22/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/588,103	MIURA, MINEO	
	Examiner	Art Unit	
	FEI FEI YEUNG LOPEZ	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 December 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6 and 7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

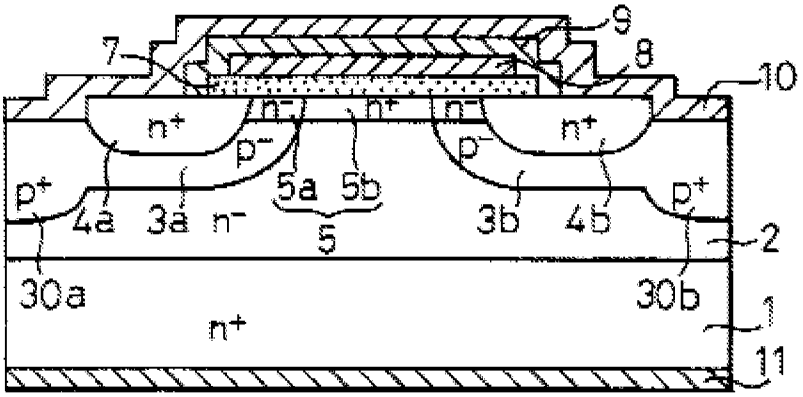
> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 6 is rejected under 35 U.S.C. 102(b) as being anticipated by Kumar et al (US Patent 6,573,534 B1).

3. Regarding claim 6, Kumar teaches a semiconductor device of a double diffused MOS structure employing a silicon carbide semiconductor substrate, the device comprising: a silicon carbide semiconductor epitaxial layer (n- layer 2 in fig. 41) provided on a surface of the silicon carbide semiconductor substrate (layer 1) and having a first conductivity (n type) which is the same conductivity as the silicon carbide semiconductor substrate; an impurity region formed by doping a surface portion of the silicon carbide semiconductor epitaxial layer with an impurity of a second conductivity (p type), the impurity region having a profile such that a near surface thereof has a relatively low second-conductivity impurity concentration (p- layer 3a and layer 3b) and a deep portion thereof has a relatively high second-conductivity impurity concentration (p+ layers 30a and 30b), wherein a second-conductivity impurity concentration (p- layer 3a) in an outermost surface portion of the impurity region is controlled to be lower than a first-conductivity impurity concentration (layer 5b) in the silicon carbide semiconductor epitaxial layer (note that the added n+ dopants compensate the p dopants in layer 3a—

the concentration of p dopants in layer 3a is less than the concentration of n dopants implanted in layer 5a. Region 5b is implanted with the same concentration of n dopants as layer 5a.) a further impurity region by doping a surface portion (layer 5a) of the impurity region of the second conductivity with an impurity of the first conductivity; and channel region (layer 5b) having the first conductivity formed in the outmost surface portion between the epitaxial layer (layer 2) and the further impurity region (layer 5a) of the first conductivity.

Fig.41



Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kumar et al (US Patent 6,573,534 B1) in view of Huang (US Patent 6,373,102 B1) and Pavlidis et al (US Patent 4,827,319).

7. Regarding claim 7, Kumar teaches a semiconductor device manufacturing method for manufacturing a semiconductor device of a double diffused MOS structure employing a silicon carbide semiconductor substrate, the method comprising steps of: forming a silicon carbide semiconductor epitaxial layer (layer 2 in fig. 41) having a first conductivity (n type) on a surface of the silicon carbide semiconductor substrate (layer 1), the first conductivity being the same conductivity as the silicon carbide semiconductor substrate; and doping a surface portion of the silicon carbide semiconductor epitaxial layer with an impurity of a second conductivity (p type) to form an impurity region having a profile such that a near surface thereof has a relatively low second-conductivity impurity concentration (layer 3a) and a deep portion thereof has a relatively high second-conductivity impurity concentration (layer 30a), wherein the surface portion of the silicon carbide semiconductor epitaxial layer is doped with the impurity of the second conductivity by single-step ion implantation (see figs. 33 and 34

and column 1, lines 48-50) in the impurity region forming step, the single-step ion implantation being performed with a single constant level of implantation energy (one temperature and one dosage concentration, see column 20, lines, and wherein a first-conductivity impurity concentration (n type layer 5b) in the epitaxial layer is higher than a second-conductivity impurity concentration (layer 3a) in an outermost surface portion of the impurity region, so as to form a channel region having the first conductivity in the outermost surface portion (of the first-conductivity impurity concentration) of the impurity region. Also, Huang teaches a layer doped by single-step ion implantation for the benefit of saving costs (column 1, lines 48-50). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to dope the surface portion of the silicon carbide semiconductor epitaxial layer with the impurity of the second conductivity by single-step ion implantation in the impurity region forming step for the benefit of saving costs. Furthermore, Pavlidis teaches ion implantation being performed with a single constant level of implantation energy (column 3, lines 52-60) for the benefit of creating a transition of doping level. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to perform the single-step ion implantation with a single constant level of implantation energy for the benefit of creating a transition of doping level.

Fig.33

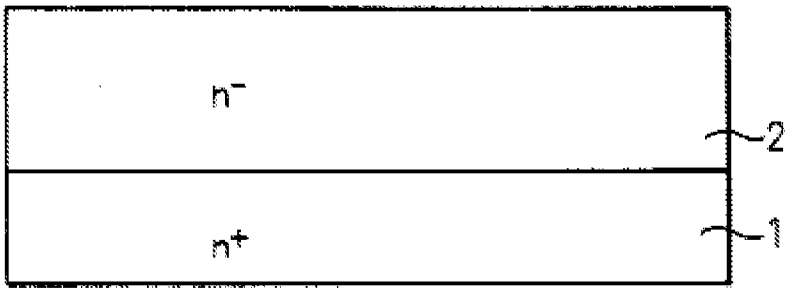
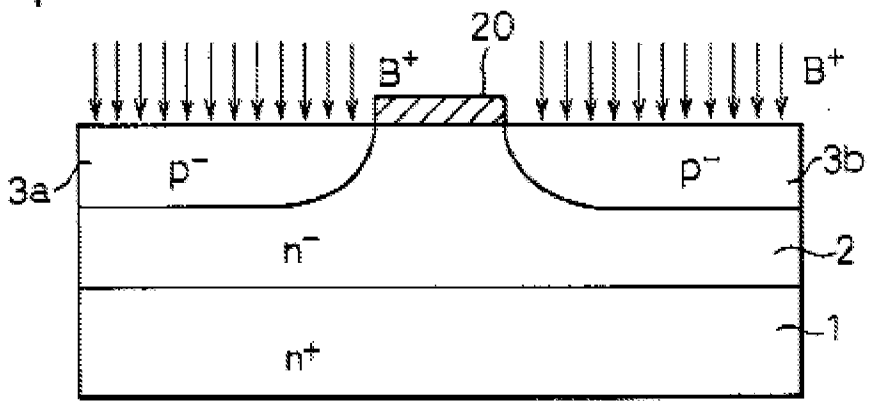


Fig.34



Response to Arguments

8. Applicant's arguments with respect to claims 6-7 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to FEI FEI YEUNG LOPEZ whose telephone number is (571)270-1882. The examiner can normally be reached on 7:30am-5:00pm Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

FYL
/Feifei Yeung-Lopez/
Examiner, Art Unit 2826

/Sue A Purvis/

Supervisory Patent Examiner, Art Unit 2826